BJ24C02
I^2C Serial EEPROM

Product Specification

Specification Revision History:

Version	Data	Description
2023-05-A1	2023-05	New

Contents

1、General Description

BJ24C02 provides 2048 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 256 words of 8 bits each. Inside is divided into 32 pages, each page 8 bytes,, Fully I^2C Bus Compatible, A random word address need a 8 bits of data word The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential.

Features:

- Write Protect Pin for Hardware Data Protection
- Wide Voltage Operation: 1.8V to 5.5V
- Internally Organized:256×8(2K)
- Two-wire Serial Interface
- Schmitt Trigger Inputs for Noise Suppression
- Bidirectional data transfer protocol
- 400KHZ(1.8V to 2.5V) and 1MHZ(2.5V to 5.5V) Compatibility
- 8-byte Page(2K)
- Partial page writes allowed
- Self-timed write cycle(5ms max)
- High-reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- Automatic a wider temperature range
- Multiple package options: DIP8/SOP8/TSSOP8

Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
BJ24C02DA8.TB	DIP8	BJ24C02	50 PCS/tube	40 tube/box	2000 PCS/box	Dimensions of plastic enclosure: 9.2mm×6.4mm Pin spacing: 2.54mm
BJ24C02SA8.TB	SOP8	BJ24C02	100 PCS/tube	100 tube/box	10000 PCS/box	Dimensions of plastic enclosure: 4.9mm×3.9mm Pin spacing: 1.27mm
BJ24C02TA8.TB	TSSOP8	BJ24C02	100 PCS/tube	200 tube/box	20000 PCS/box	Dimensions of plastic enclosure: 4.4mm×3.0mm Pin spacing: 0.65mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
BJ24C02SA8.TR	SOP8	BJ24C02	4000PCS/reel	8000PCS/box	Dimensions of plastic enclosure: 4.9mm×3.9mm Pin spacing: 1.27mm
BJ24C02TA8.TR	TSSOP8	BJ24C02	3000PCS/reel	3000PCS/box	Dimensions of plastic enclosure: 4.4mm×3.0mm Pin spacing: 0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

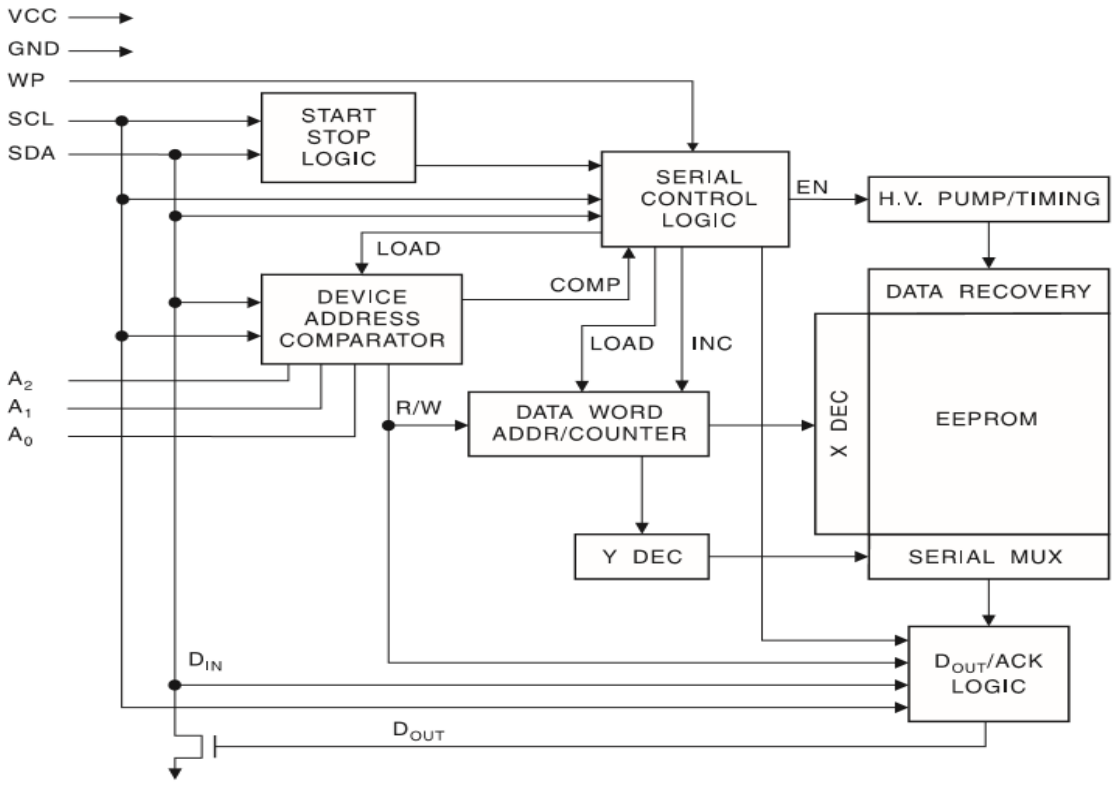


Figure 1. Block Diagram

2.2、Pin Configurations

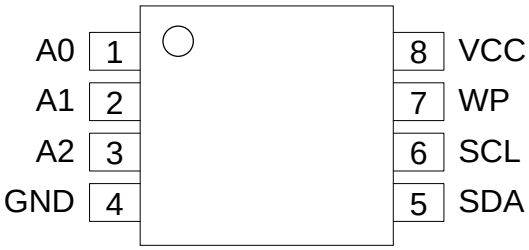


Figure 2. Pin configuration

2.3、Pin Description

<table>
<tr><th>Pin name</th><th>Symbol</th><th>Description</th></tr>
<tr><td>1</td><td>A0</td><td rowspan="3">The A2, A1 and A0 pins are device address inputs that are hard wired for the BJ24C02.As many as eight 2K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).</td></tr>
<tr><td>2</td><td>A1</td></tr>
<tr><td>3</td><td>A2</td></tr>
<tr><td>4</td><td>GND</td><td>Circuit ground pin.</td></tr>
<tr><td>5</td><td>SDA</td><td>The SDA pin is bidirectional for serial data transfer.This pin is open-drain and may be wire-Ored with any number of other open-drain or open-collector devices.</td></tr>
<tr><td>6</td><td>SCL</td><td>The SCL input is used to position edge clock data into each EEPROM device and negation edge clock data out of each device.</td></tr>
<tr><td>7</td><td>WP</td><td>Write protect.:The WP pin that provides hardware data protection. The WP pin allows normal read/write operations when connected to ground (GND). When the WP pin is connected to VCC, the write protection feature is enabled and read only.
<table>
<tr><td>WP Pin status</td><td>Part of the Array Protected</td></tr>
<tr><td>At VCC</td><td>Full(2K)</td></tr>
<tr><td>At GND</td><td>Normal Read/Write Operations</td></tr>
</table></td></tr>
<tr><td>8</td><td>VCC</td><td>Positive supply voltage</td></tr>
</table>

3、Electrical Parameter

3.1、Absolute Maximum Ratings

(T_{amb}=25℃, unless otherwise specified)

Characteristic	Symbol	Conditions		Value	Unit
Power Supply Voltage	VCC	-		6.25 (max)	V
DC output current	I	-		5.0	mA
Any pins relatively voltage	V	-		-1.0 to +7.0	V
Input/output capacitance(SDA)	$C_{I/O}$	T_{amb}=25℃, f=1.0MHz, VCC=+1.8V,$V_{I/O}$=0V,note 1		8 (max)	pF
Input capacitance (A0,A1,A2,SCL)	C_{IN}	T_{amb}=25℃, f=1.0MHz, VCC=+1.8V,V_{IN}=0V,note 1		6 (max)	pF
Operating ambient temperature	T_{amb}	-		-40 to +85	℃
storage temperature	T_{stg}	-		-65 to +150	℃
Soldering Temperature	T_L	10s	DIP	250	℃
			SOP/TSSOP	260	

Note:

1. The characteristic value of these parameters is not 100% measured values.

2. Device more than limit the scope of use can lead to device permanently damaged, the scope is the main scope, not including other not mentioned. For a long time in a value will influence on the reliability of the device.

3.2、Electrical Characteristics

3.2.1、DC Characteristics

(T_{amb}=-40 to +85℃, VCC=+1.8 to +5.5V, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	VCC	-	1.8	-	5.5	V
Supply current	I_{CCR}	VCC=5.5V, Read at 400kHz	-	0.2	0.4	mA
Supply current	I_{CCW}	VCC=5.5V, Write at 400kHz	-	0.8	1.6	mA
Standby current	I_{SB1}	VCC=3.3V, V_{IN}=VCC or VSS	-	-	1.0	uA
Standby current	I_{SB2}	VCC=5.5V, V_{IN}=VCC or VSS	-	-	3.0	uA
Input leakage current	I_{LI}	V_{IN}=VCC or VSS	-	0.10	1.0	uA
Output leakage current	I_{LO}	V_{OUT}=VCC or VSS	-	0.05	1.0	uA
Input low level	V_{IL}	-	-0.6	-	0.3VCC	V
Input high level	V_{IH}	-	0.7VCC	-	VCC+0.3	V
Output low level	V_{OL2}	I_{OL}=2.1mA, VCC=3.0V	-	-	0.4	V
Output low level	V_{OL1}	I_{OL}=1.5mA, VCC=1.8V	-	-	0.2	V

Note: V_{IL} min and V_{IH} max are reference only and not tested.

3.2.2、AC Characteristics

((T_{amb}=-40 to +85℃, VCC=+1.8V to +5.5V, C_L=1TTL Gate and 100pF, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Clock Frequency, SCL	f_{SCL}	VCC=1.8V	-	-	100	kHz
		VCC=2.7V	-	-	400	
		VCC=5.0V	-	-	1000	
Clock Pulse Width Low	t_{LOW}	VCC=1.8V	1.3	-	-	us
		VCC=2.7V	0.4	-	-	
		VCC=5.0V	0.4	-	-	
Clock Pulse Width High	t_{HIGH}	VCC=1.8V	0.6	-	-	us
		VCC=2.7V	0.4	-	-	
		VCC=5.0V	0.4	-	-	
Noise Suppression Time	t_I	VCC=1.8V	-	-	100	ns
		VCC=2.7V	-	-	50	
		VCC=5.0V	-	-	50	
Clock Low to Data Out Valid	t_{AA}	VCC=1.8V	0.05	-	0.9	us
		VCC=2.7V	0.05	-	0.55	
		VCC=5.0V	0.05	-	0.55	
Time the bus must be free before a new transmission can start	t_{BUF}	VCC=1.8V	1.3	-	-	us
		VCC=2.7V	0.5	-	-	
		VCC=5.0V	0.5	-	-	
Start Hold Time	$t_{HD.STA}$	VCC=1.8V	0.6	-	-	us
		VCC=2.7V	0.25	-	-	
		VCC=5.0V	0.25	-	-	
Start Setup Time	$t_{SU.STA}$	VCC=1.8V	0.6	-	-	us
		VCC=2.7V	0.25	-	-	

		VCC=5.0V	0.25	-	-	
Data In Hold Time	$t_{HD.D}$	VCC=1.8V	0	-	-	us
		VCC=2.7V	0	-	-	
		VCC=5.0V	0	-	-	
Data In Setup Time	$t_{SU.D}$	VCC=1.8V	100	-	-	ns
		VCC=2.7V	100	-	-	
		VCC=5.0V	100	-	-	
Inputs Rise Time	t_R	VCC=1.8V	-	-	0.3	us
		VCC=2.7V	-	-	0.3	
		VCC=5.0V	-	-	0.3	
Inputs Fall Time	t_F	VCC=1.8V	-	-	300	ns
		VCC=2.7V	-	-	100	
		VCC=5.0V	-	-	100	
Stop Setup Time	$t_{SU.STO}$	VCC=1.8V	0.6	-	-	us
		VCC=2.7V	0.25	-	-	
		VCC=5.0V	0.25	-	-	
Data Out Hold Time	t_{DH}	VCC=1.8V	50	-	-	ns
		VCC=2.7V	50	-	-	
		VCC=5.0V	50	-	-	
Write Cycle Time	t_{WR}	VCC=1.8V	-	-	5	ms
		VCC=2.7V	-	-	5	
		VCC=5.0V	-	-	5	
Byte mode	endurance	VCC=5.0V T_{amb}=25℃	VCC=1.8V	100M	-	-	Write cycles
			VCC=2.7V	100M	-	-	
			VCC=5.0V	100M	-	-	

Note: This parameter is characterized

4、Function Description

4.1、Device Operation

4.1.1、Clock and data transitions:

The SDA pin is normally pulled high with an external device .Data on the SDA pin may change only during SCL low time periods(see Figure 3).Data changes during SCL high periods will indicate a start or stop condition as defined below.

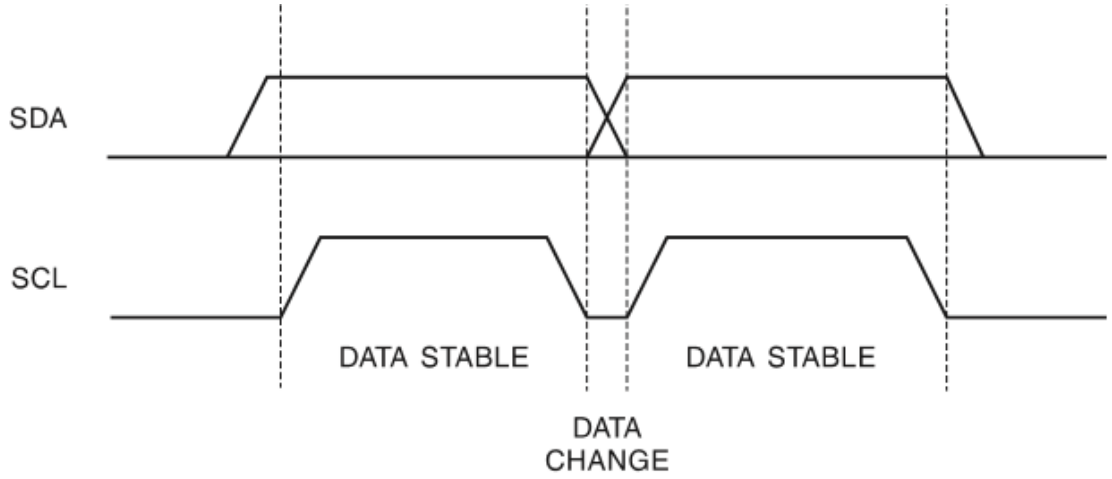


Figure 3. Data validity

4.1.2、Start Condition

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command, see Figure4.

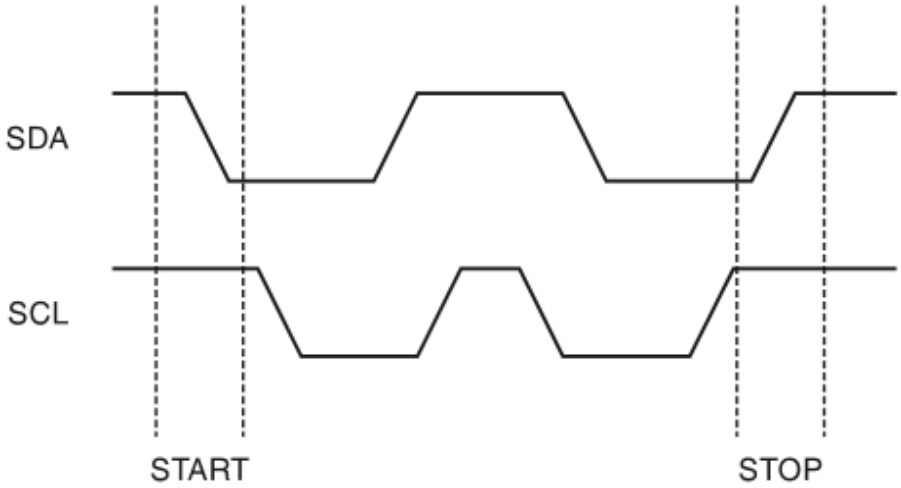


Figure 4. Start and Stop Definition

4.1.3、Stop Condition

A low -to-low transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode, see Figure4.

4.1.4、Acknowledge

All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

4.1.5、Standby Mode

The BJ24C02 features a low-power standby mode which is enabled: (a)upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations.

4.1.6、Memory Reset

After an interruption in protocol, power loss or system reset, any 2-wire part can be reset by reset by following these steps:

1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high.
3. Create a start condition while SCL is high.

4.1.7、SERIAL

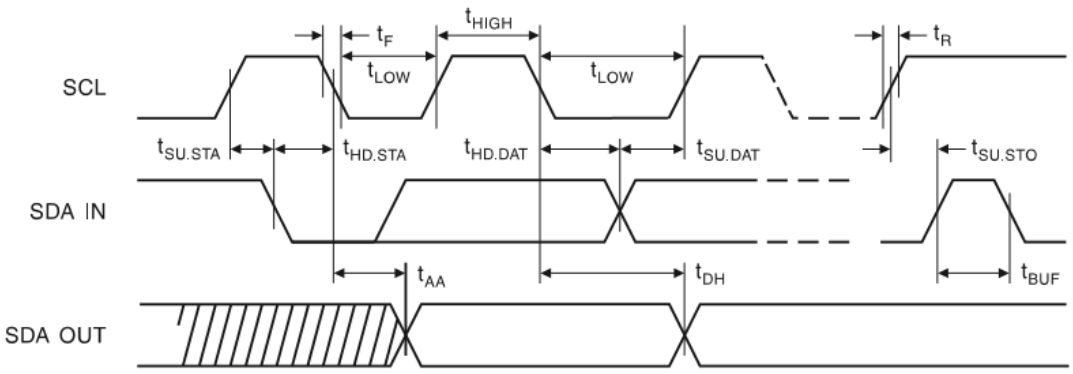
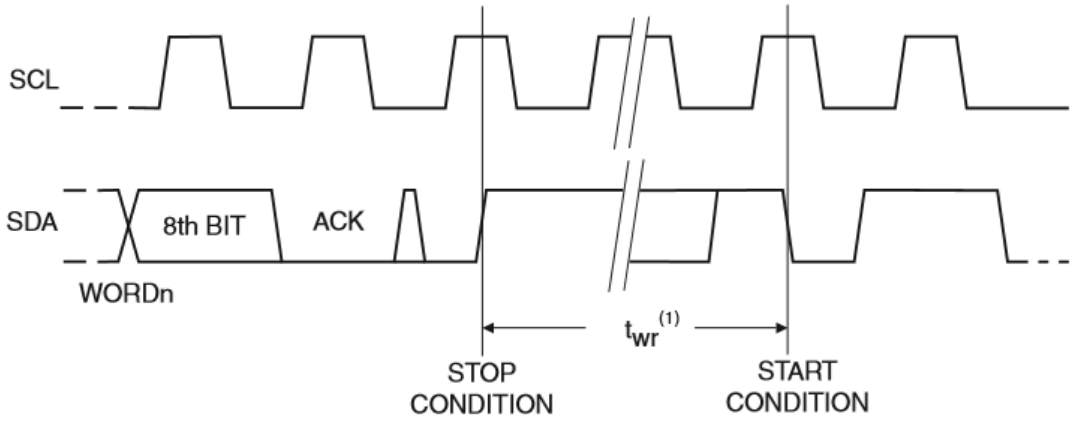


Figure 5. Bus Timing



Note: The cycle time t_{WR} is the time from a valid stop condition of a write sequence to the end of internal clear/write cycle.

Figure 6. Write Cycle Timing

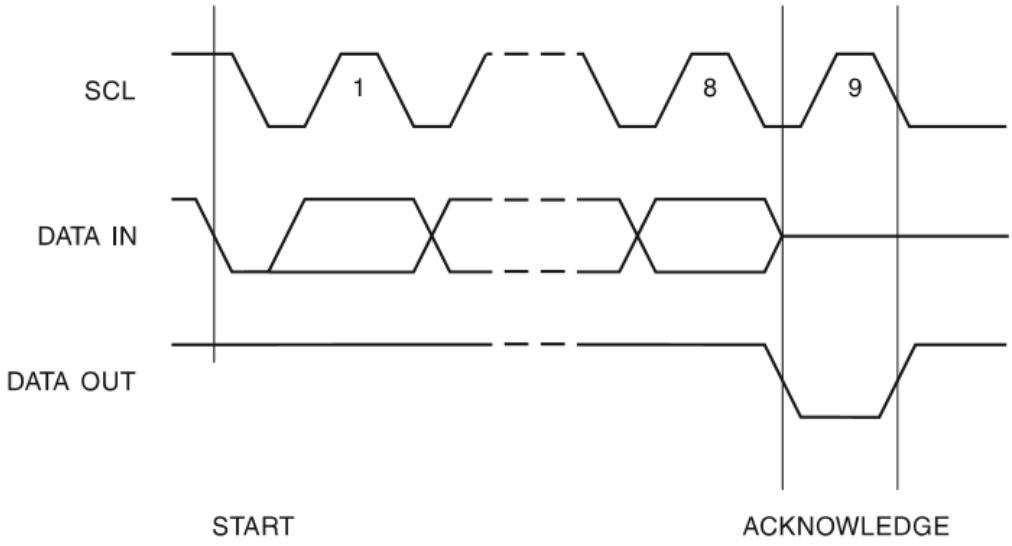


Figure 7. Output Acknowledge

4.2、Device Addressing

The EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation, shown in the following table.

MSB							LSB
1	0	1	0	A2	A1	A0	R/W

The device address word consists of a mandatory "1", "0" sequence for the first four most significant bits as shown.

The next 3 bits are the A2, A1 and A0 device address bits.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a "0". If a compare is not made, the chip will return to a standby state.

4.3、Write Operation

4.3.1、Byte Write:

A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete，see Figure 8.

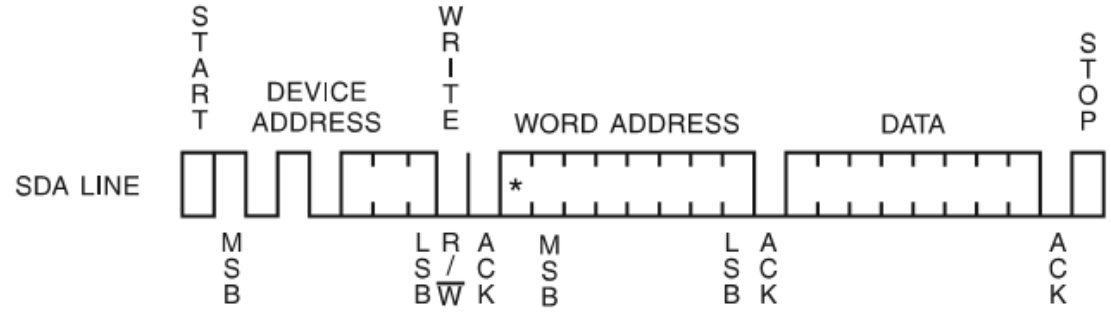


Figure 8. Byte Write

4.3.2、Page Write

The BJ24C02 device is capable of an 8-byte page write. A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 7 more data words. The EEPROM will respond with a "0" after each data word received.

The microcontroller must terminate the page write sequence with a stop condition, see Figure 9.

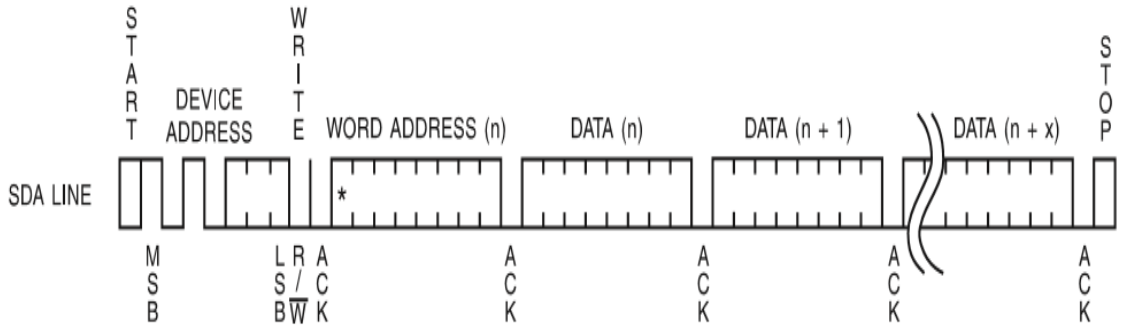


Figure 9. Page Write

The data word address lower 3 bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 8 data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

4.3.3、Acknowledge Polling

Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowing the read or write sequence to continue.

4.4、Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: current address read, random address read and sequential read.

4.4.1、Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition, see Figure 10.

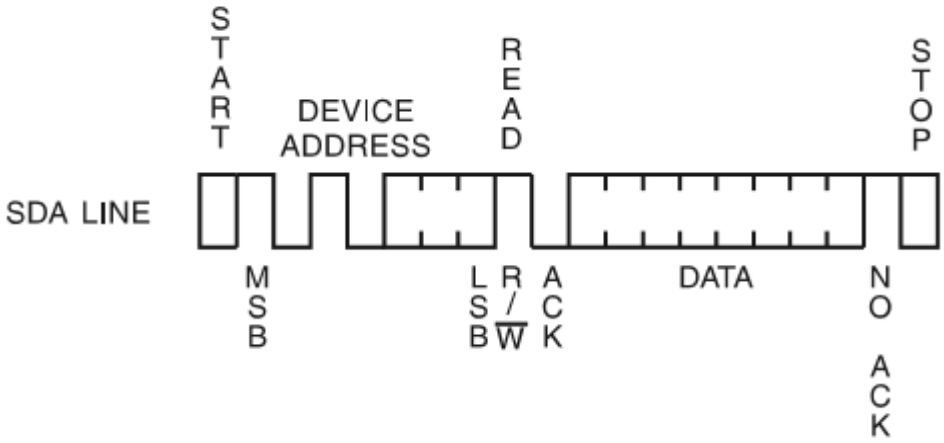


Figure 10. Current Address Read

4.4.2、Random Address Read

A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition, see Figure 11.

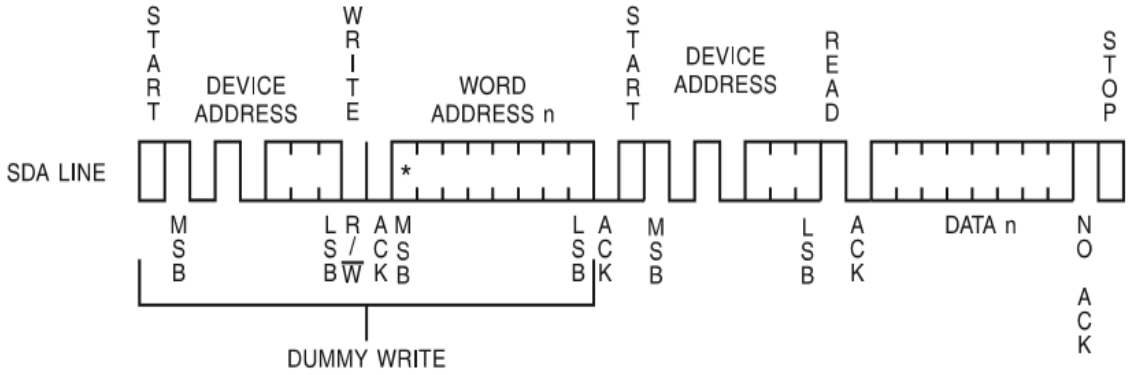


Figure 11. Random Address Read

4.4.3、Sequential Read

Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledgement. As long as the EEPROM receives an acknowledgement, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition, see Figure 12.

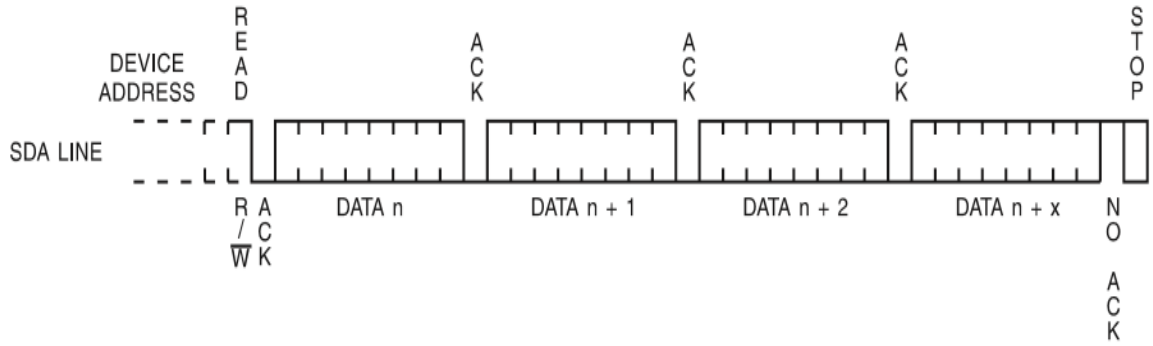
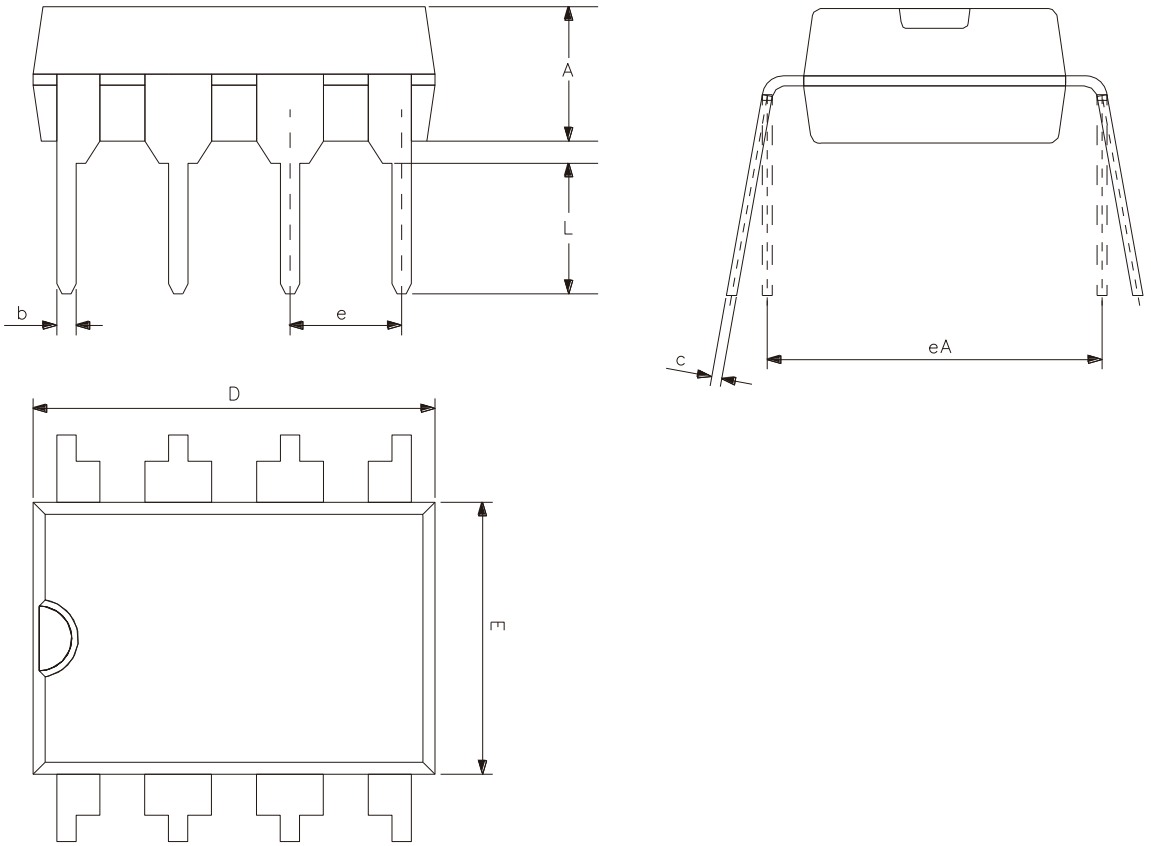


Figure 12. Sequential Read

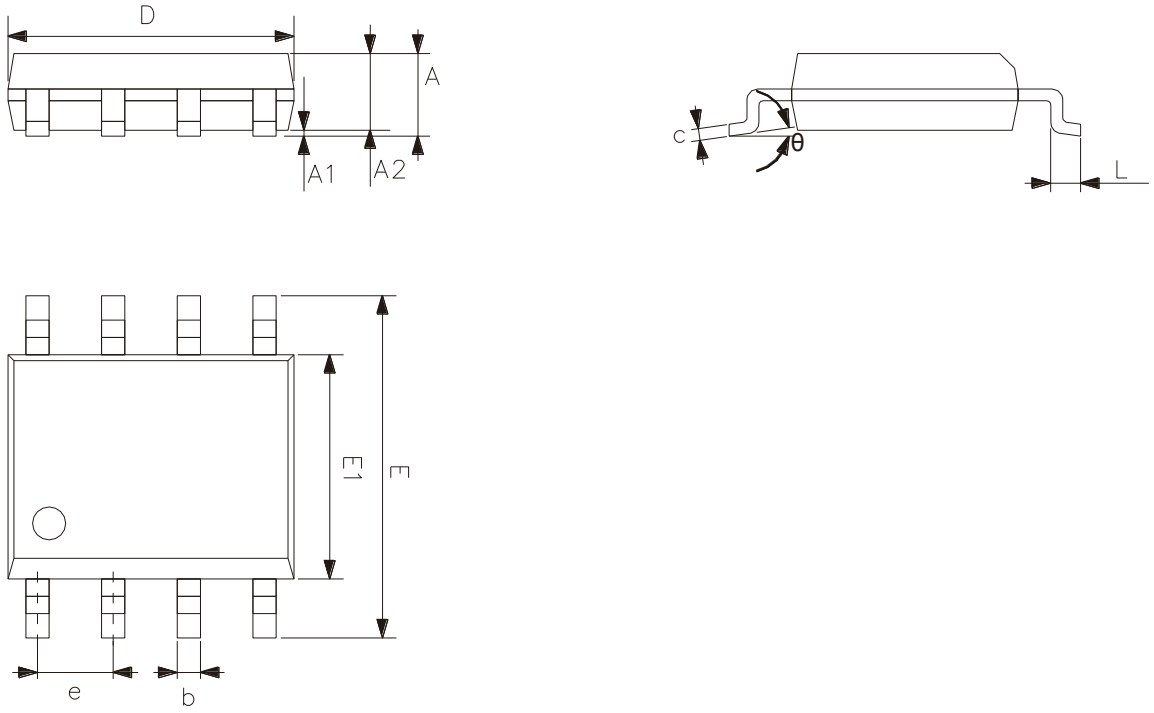
5、Package Information

5.1、DIP8



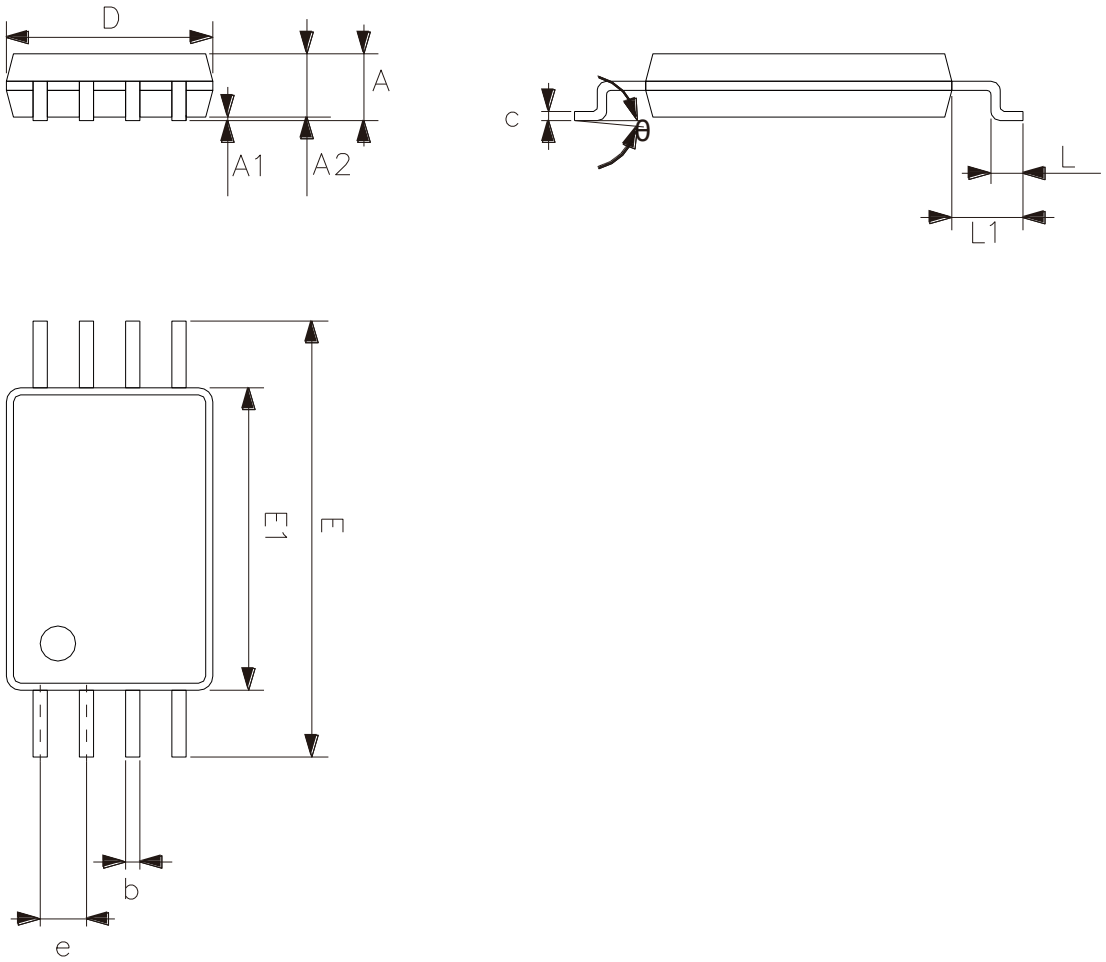
Symbol	Dimensions (mm)	
	Min.	Max.
A	3.00	3.60
b	0.36	0.56
c	0.20	0.36
D	9.00	9.45
E	6.15	6.60
e	2.54	
eA	7.62	9.30
L	3.00	-

5.2、SOP8



Symbol	Dimensions (mm)	
	Min.	Max.
A	1.35	1.80
A1	0.05	0.25
A2	1.25	1.55
D	4.70	5.10
E	5.80	6.30
E1	3.70	4.10
b	0.306	0.51
c	0.19	0.25
e	1.27	
L	0.40	0.89
θ	0 °	8 °

5.3、TSSOP8



Symbol	Dimensions (mm)	
	Min.	Max.
A	-	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E1	4.30	4.50
E	6.20	6.60
e	0.65	
L	0.45	0.75
L1	1.00	
θ	0°	8°

6、Statements And Notes

6.1、The name and content of Hazardous substances or Elements in the product

Part name	Hazardous substances or Elements									
	Lead and lead compounds	Mercury and mercury compounds	Cadmium and cadmium compounds	Hexavalent chromium compounds	Polybrominated biphenyls	Polybrominated biphenyl ethers	Dibutyl phthalate	Butylbenzyl phthalate	Di-2-ethylhexyl phthalate	Diisobutyl phthalate
Lead frame	○	○	○	○	○	○	○	○	○	○
Plastic resin	○	○	○	○	○	○	○	○	○	○
Chip	○	○	○	○	○	○	○	○	○	○
The lead	○	○	○	○	○	○	○	○	○	○
Plastic sheet installed	○	○	○	○	○	○	○	○	○	○
explanation	○：Indicates that the content of hazardous substances or elements in the detection limit of the following the SJ/T11363-2006 standard. ×：Indicates that the content of hazardous substances or elements exceeding the SJ/T11363-2006 Standard limit requirements.									

6.2、Notes

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